

FIG. 1

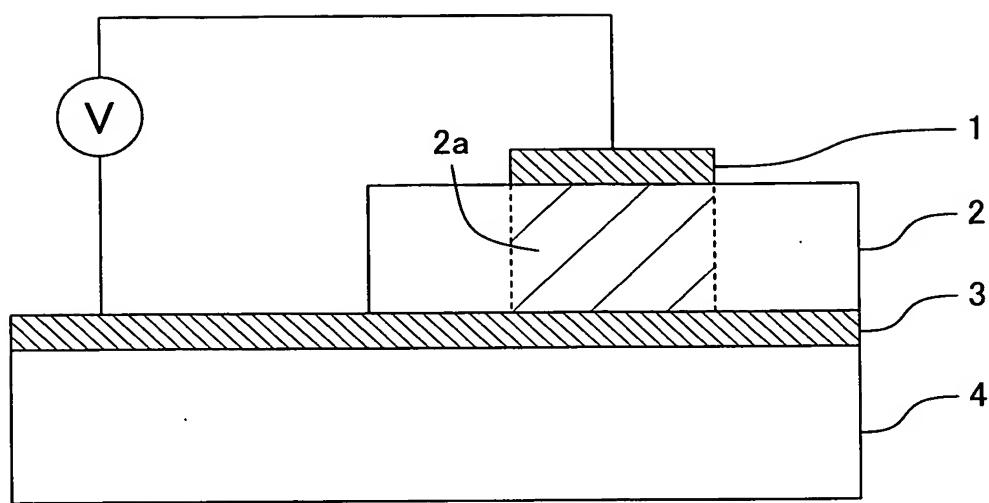


FIG. 2

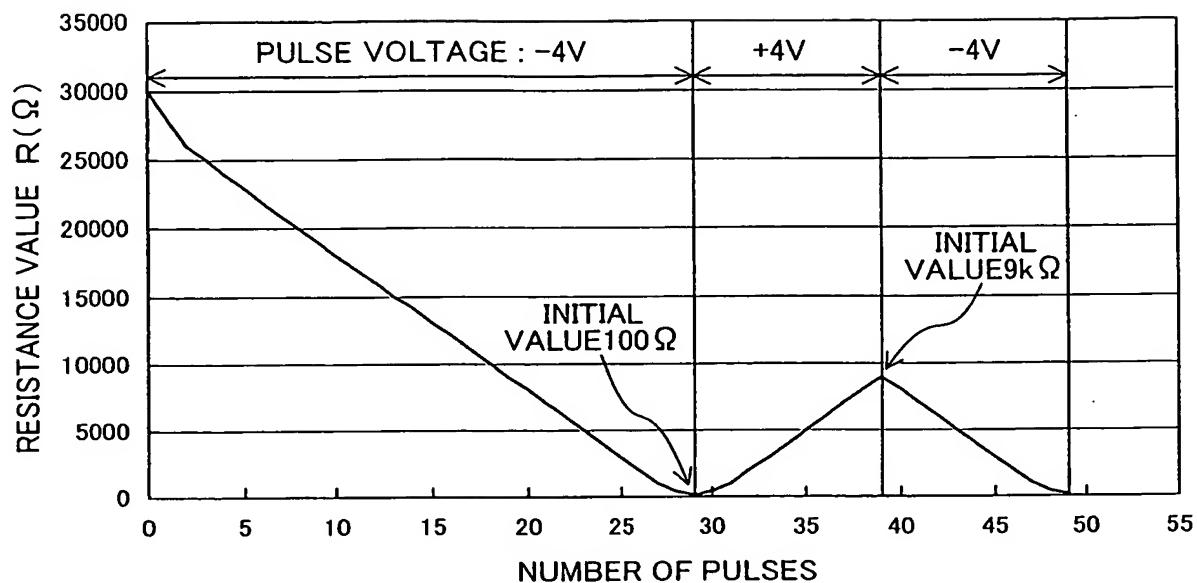
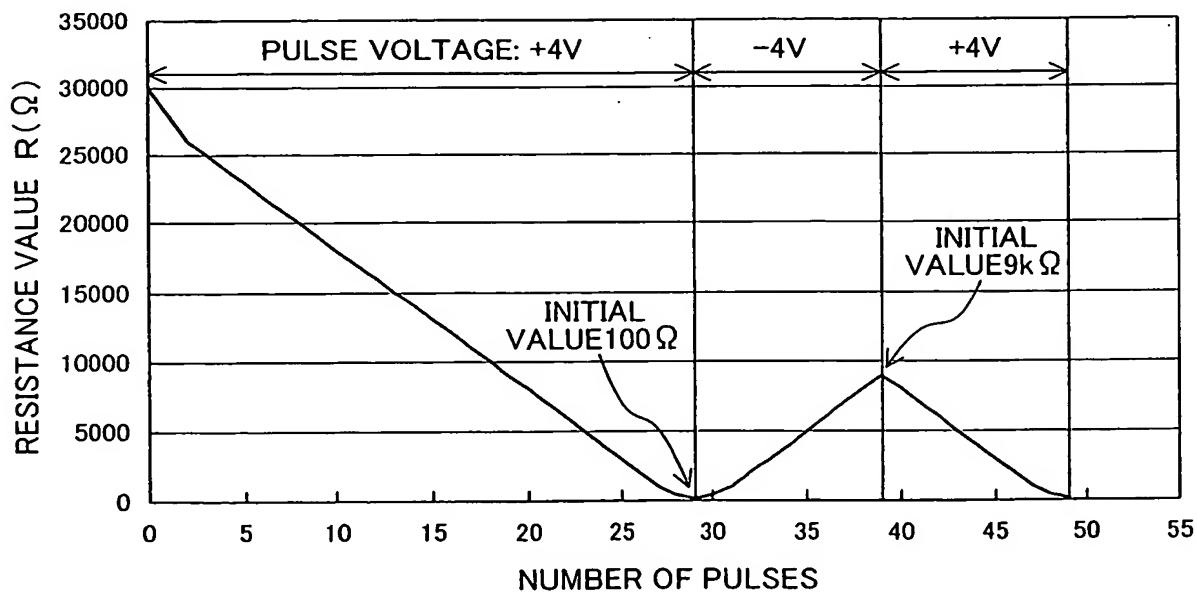
(a) VARIABLE RESISTOR α (b) VARIABLE RESISTOR β 

FIG. 3

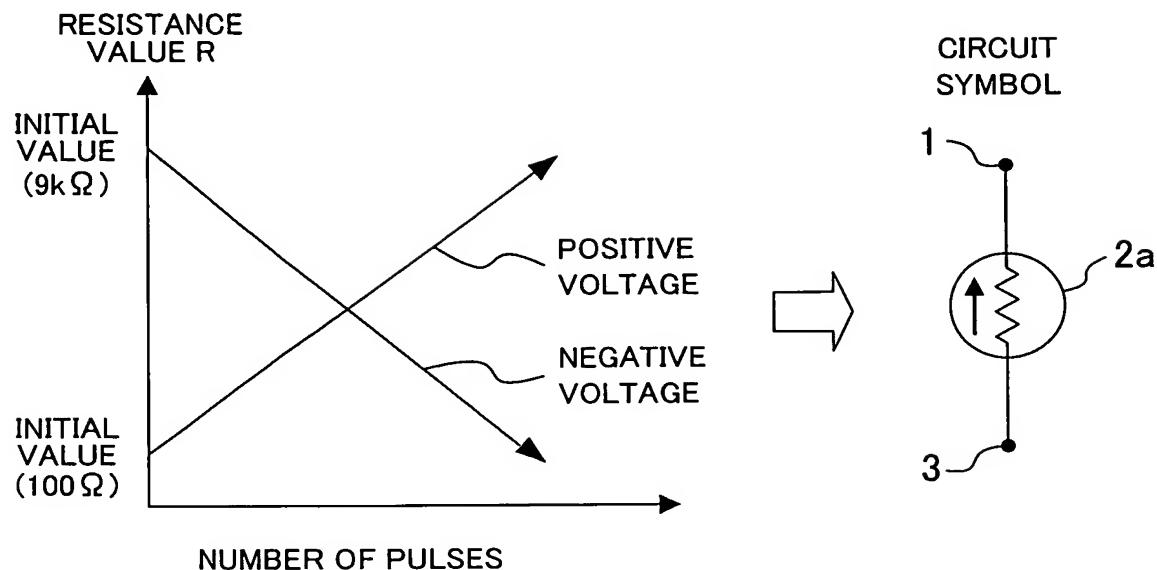
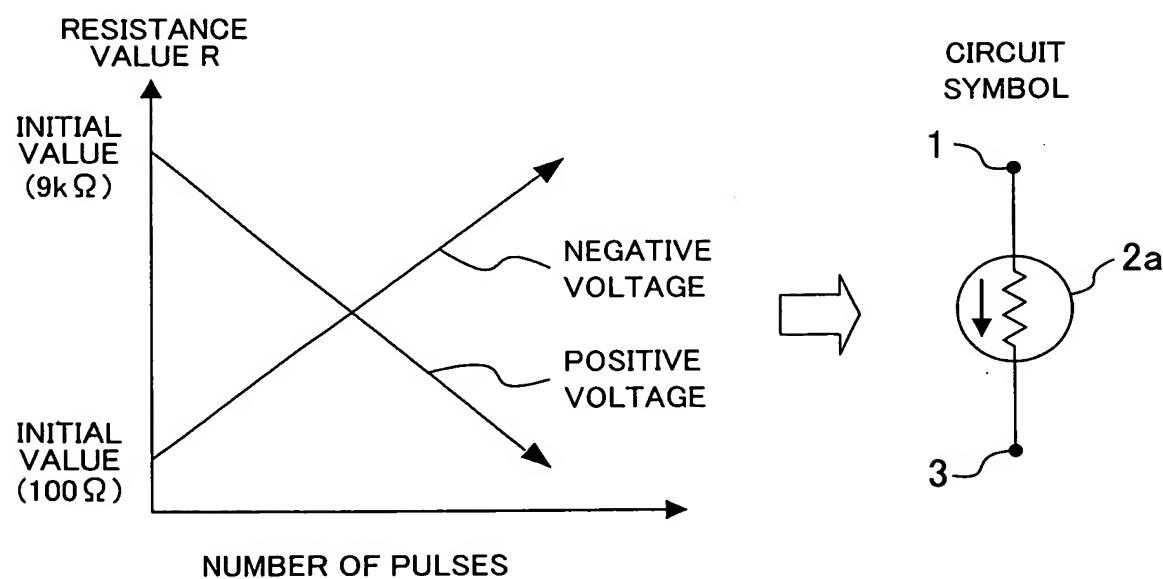
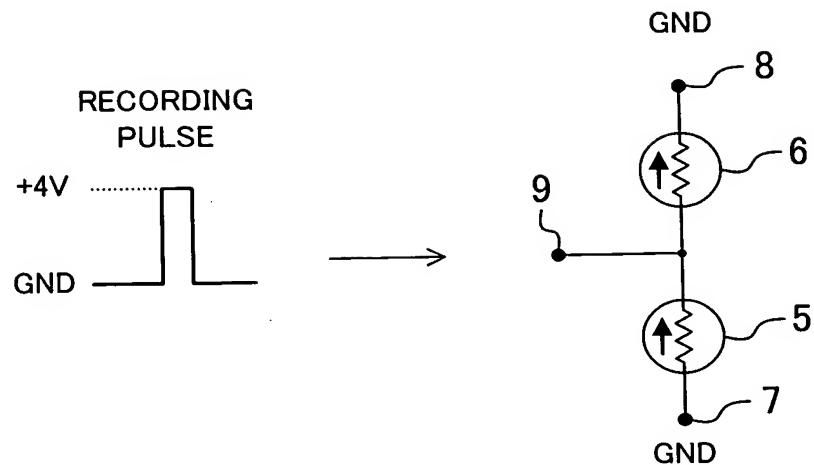
(a) VARIABLE RESISTOR α (b) VARIABLE RESISTOR β 

FIG. 4

(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR

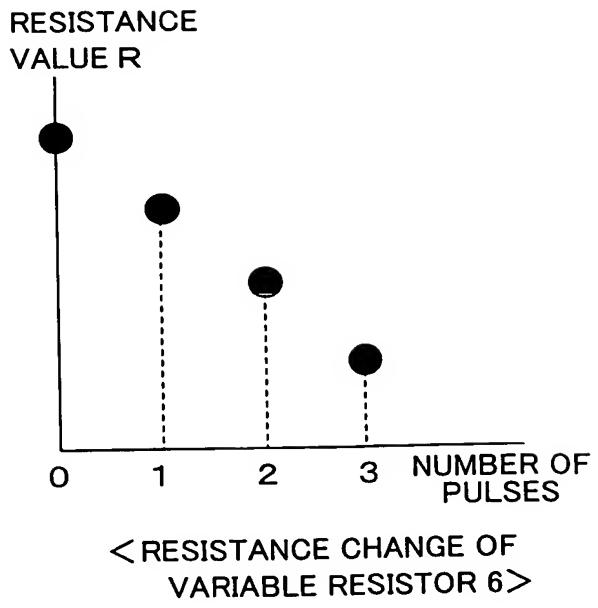
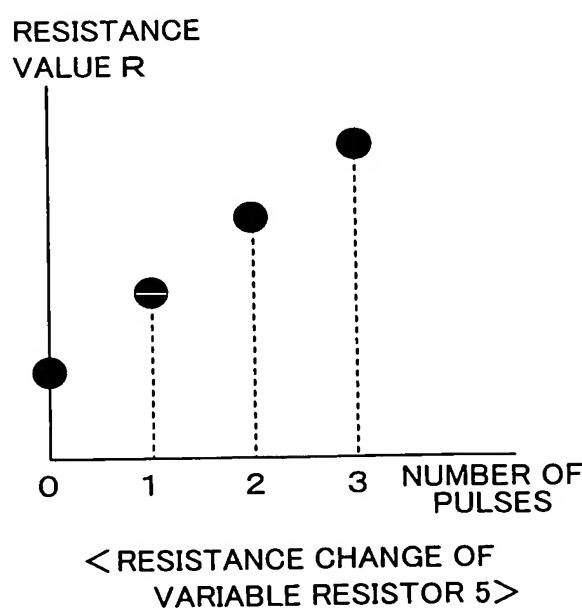
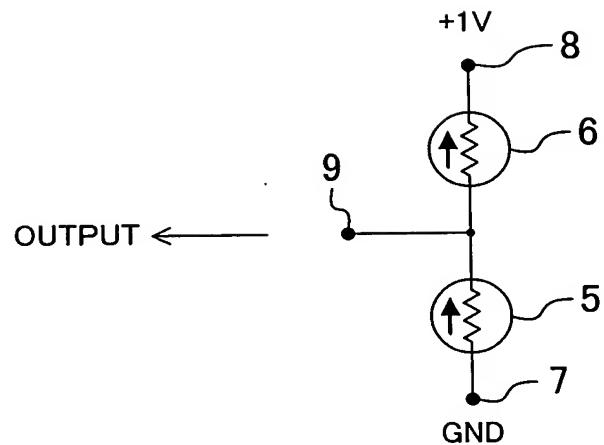


FIG. 5

(a) REPRODUCTION



(b) REPRODUCTION OUTPUT VOLTAGE

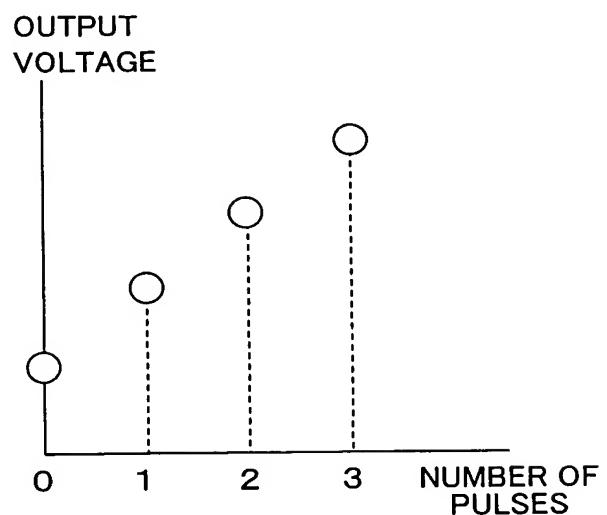
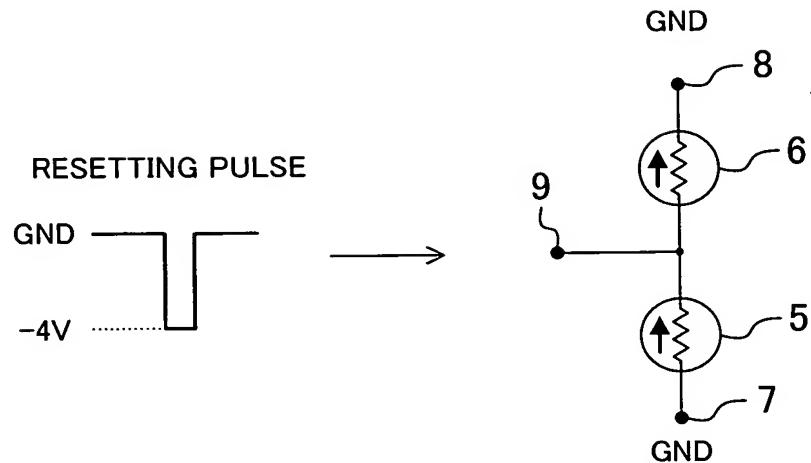
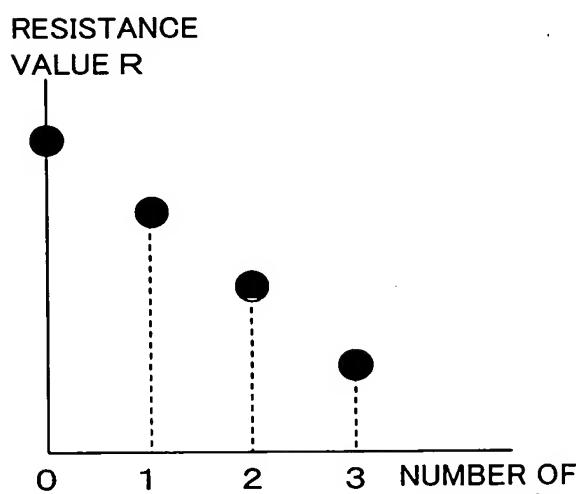


FIG. 6

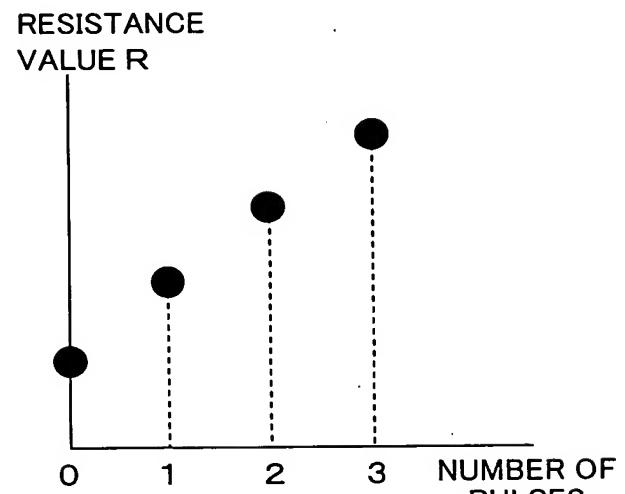
(a) RESETTING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR



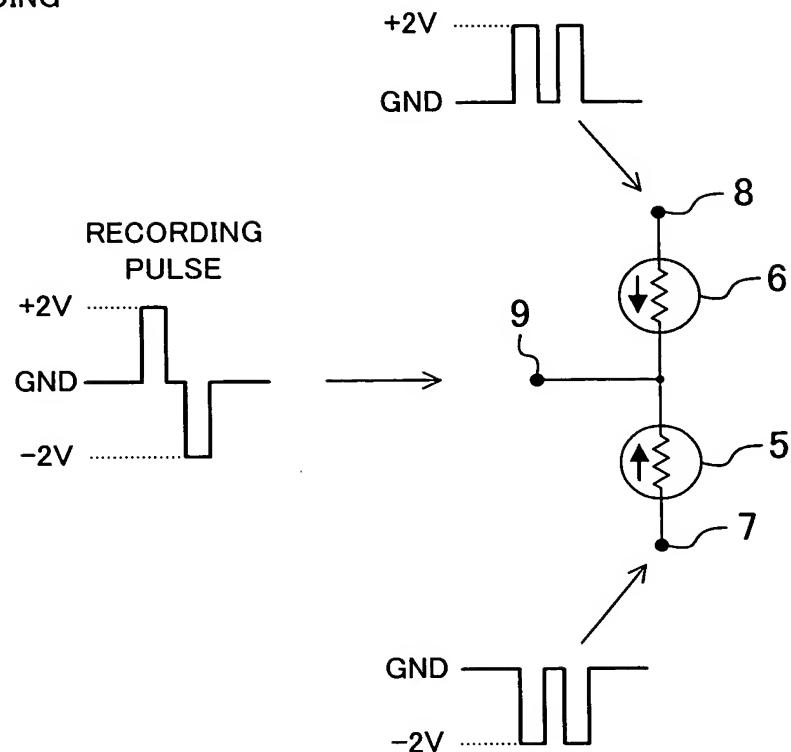
<RESISTANCE CHANGE OF VARIABLE RESISTOR 5>



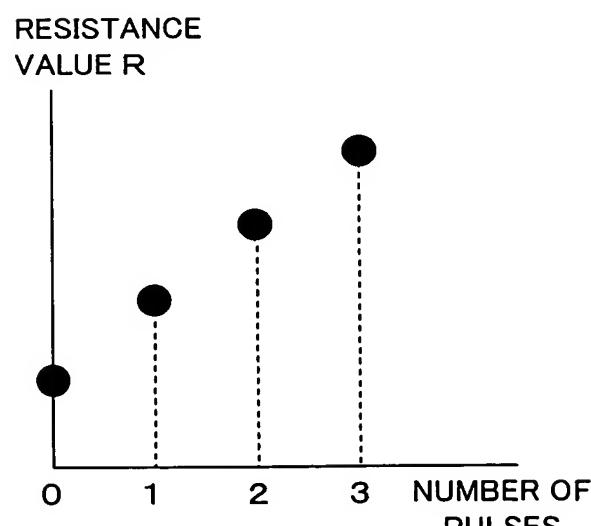
<RESISTANCE CHANGE OF VARIABLE RESISTOR 6>

FIG. 7

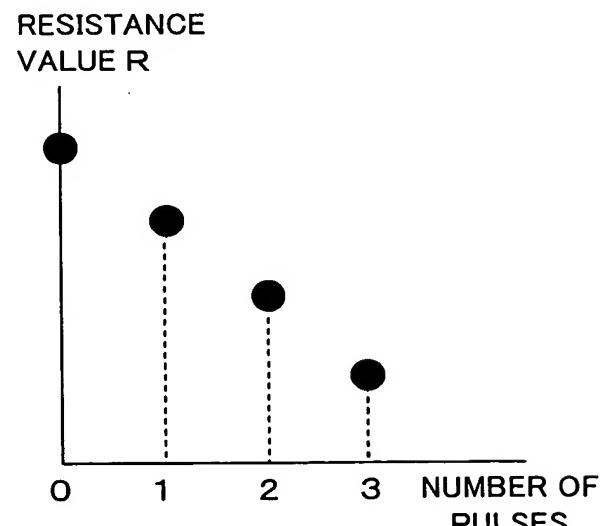
(a) RECORDING



(b) RESISTANCE CHANGE OF VARIABLE RESISTOR



<RESISTANCE CHANGE OF VARIABLE RESISTOR 5>



<RESISTANCE CHANGE OF VARIABLE RESISTOR 6>

FIG. 8

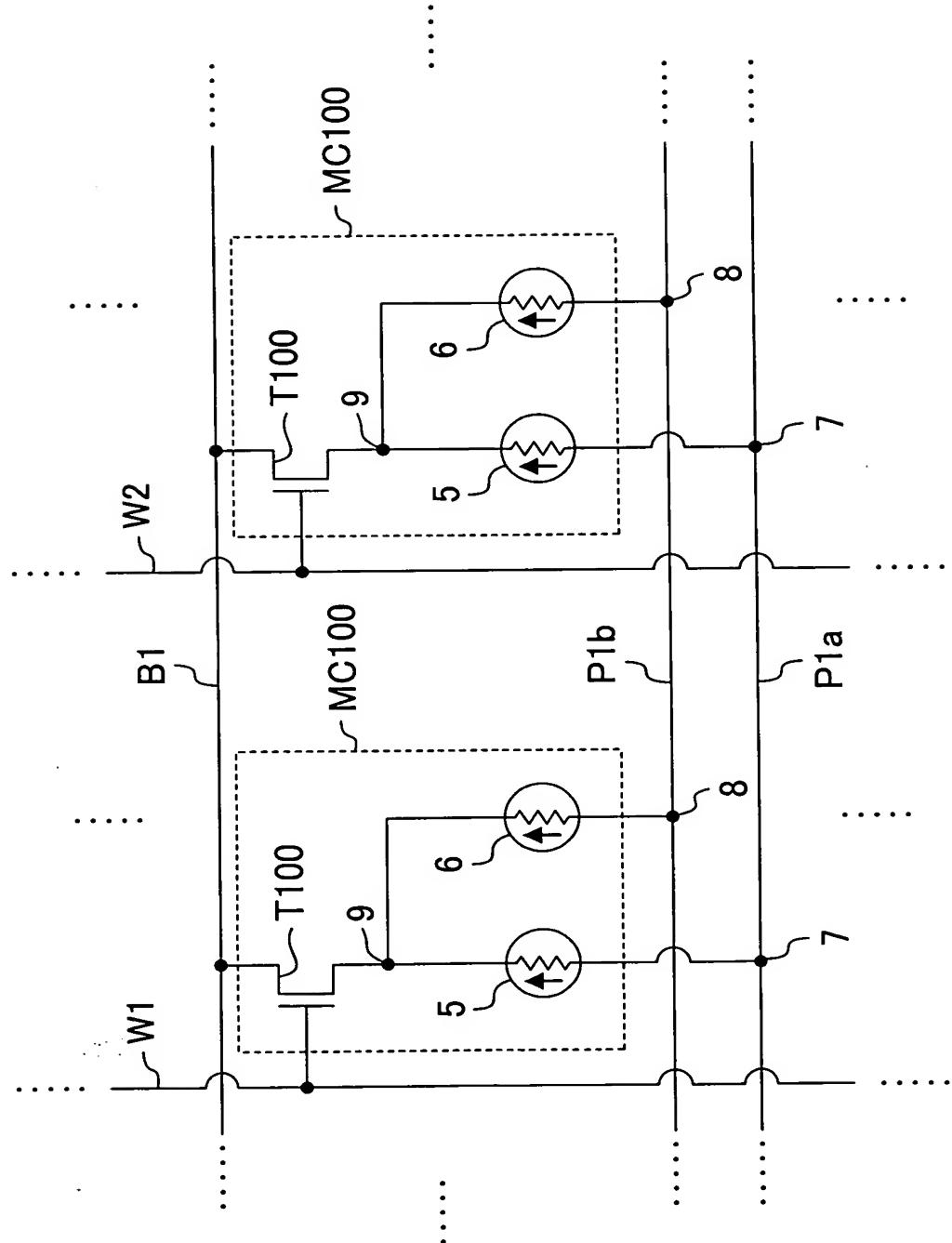


FIG. 9

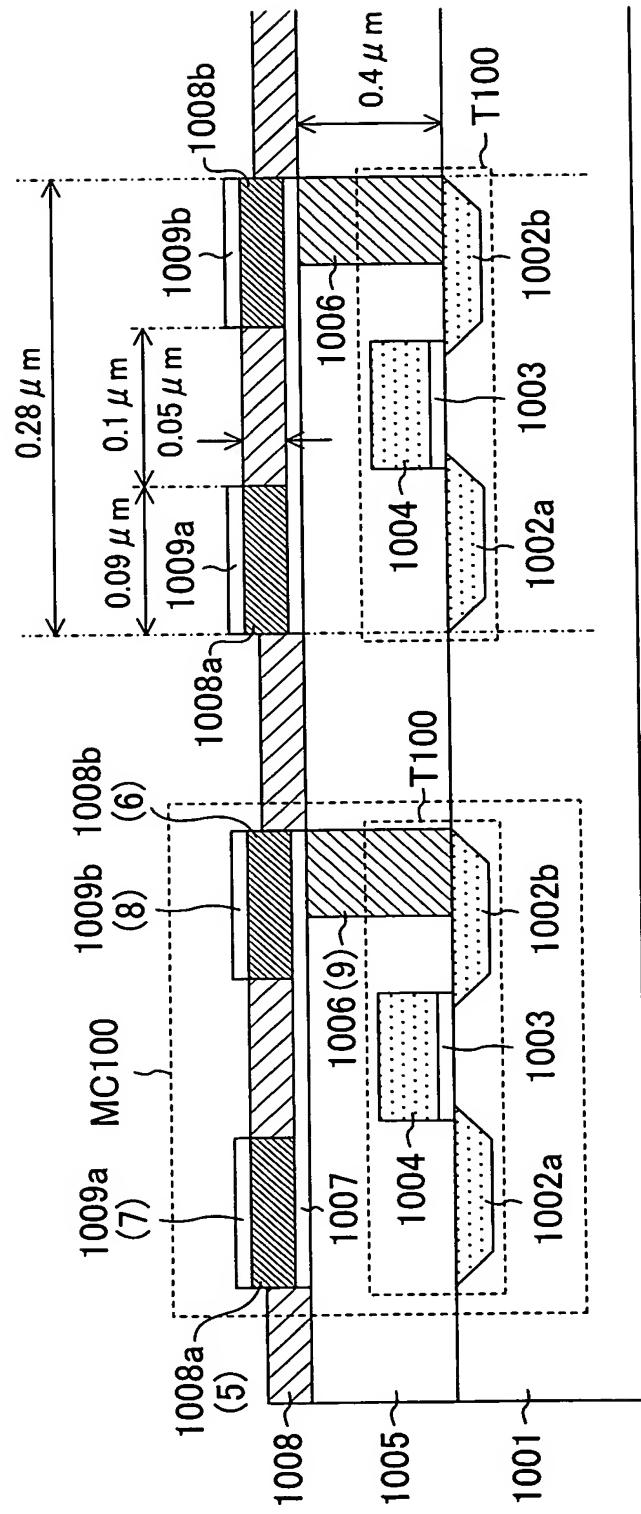
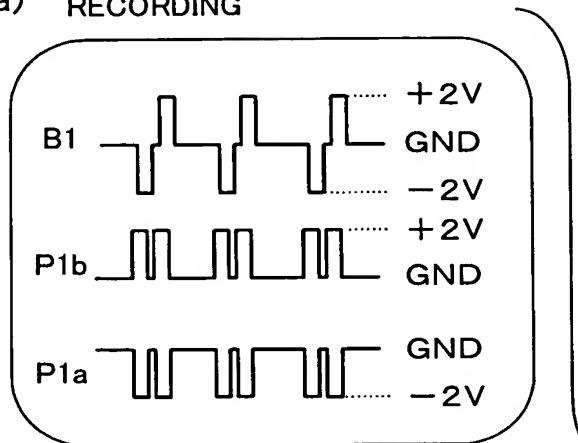
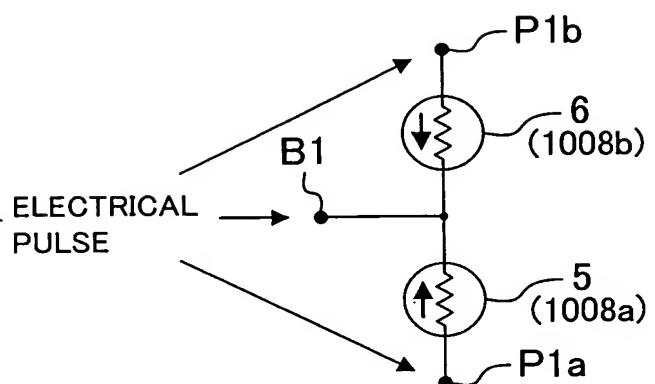
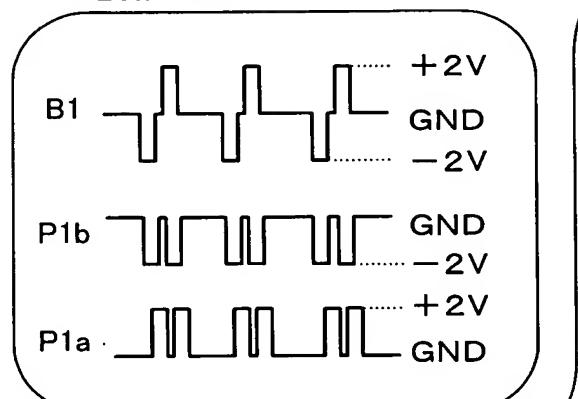


FIG. 10

(a) RECORDING



RESETTING



(b)

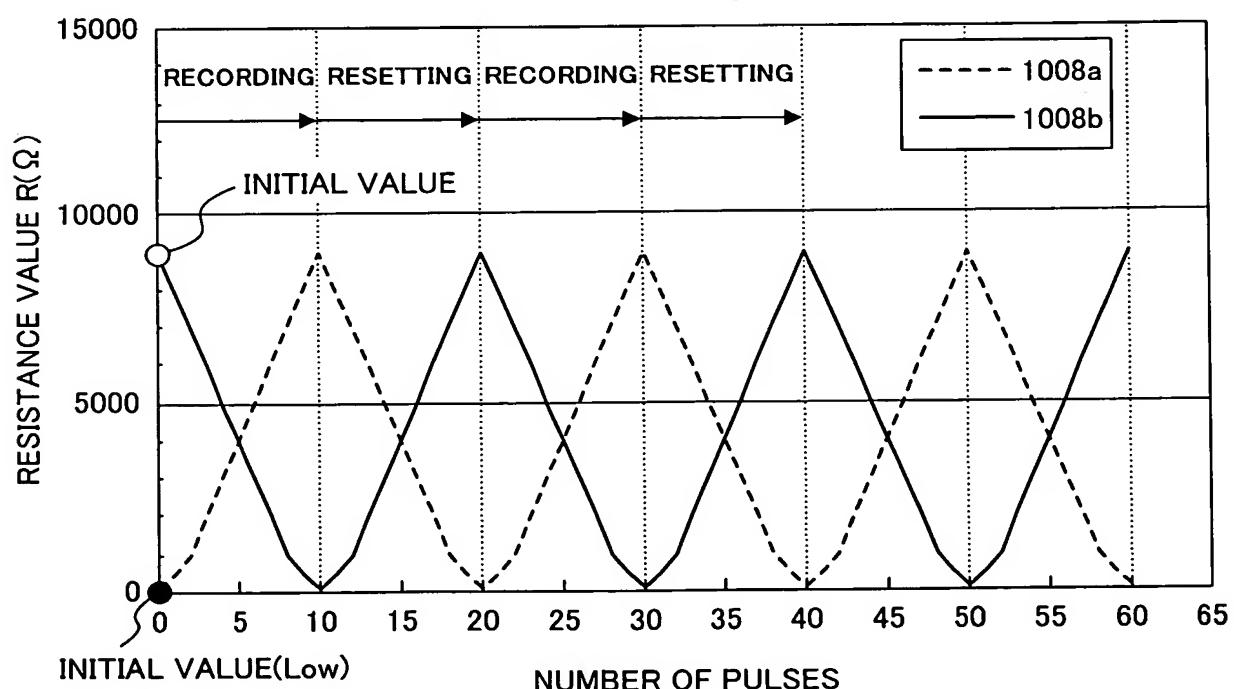
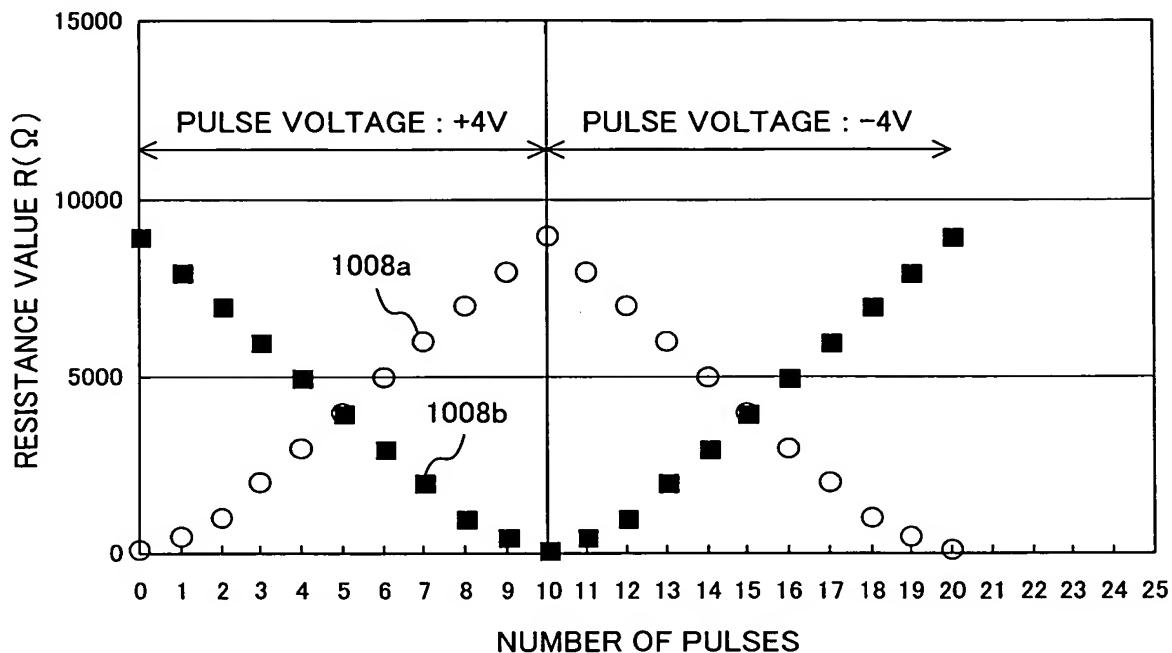


FIG. 11

(a) RESISTANCE CHANGE WITH NUMBER OF PULSES



(b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

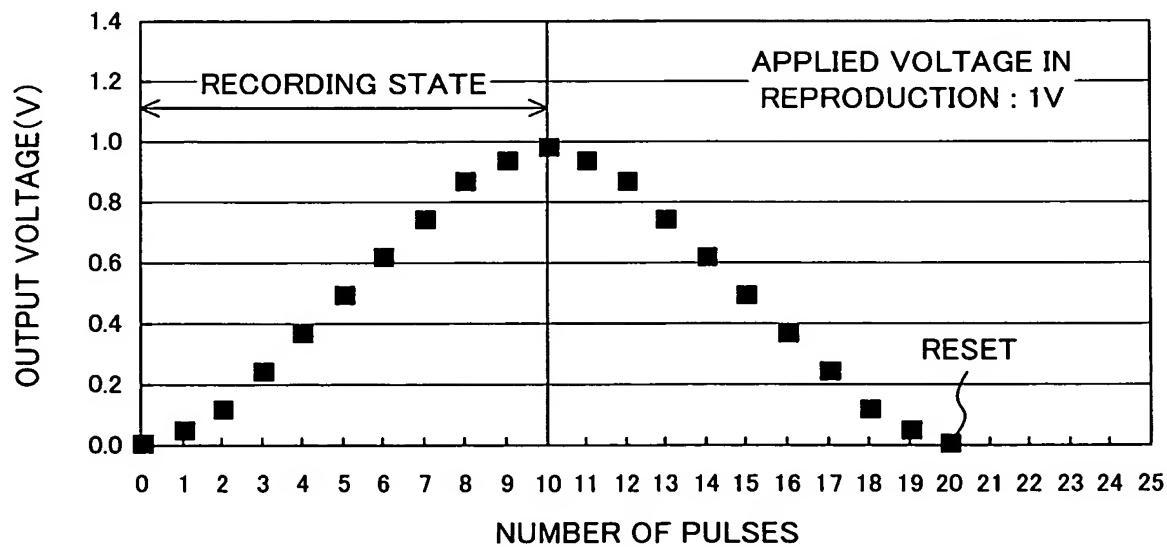
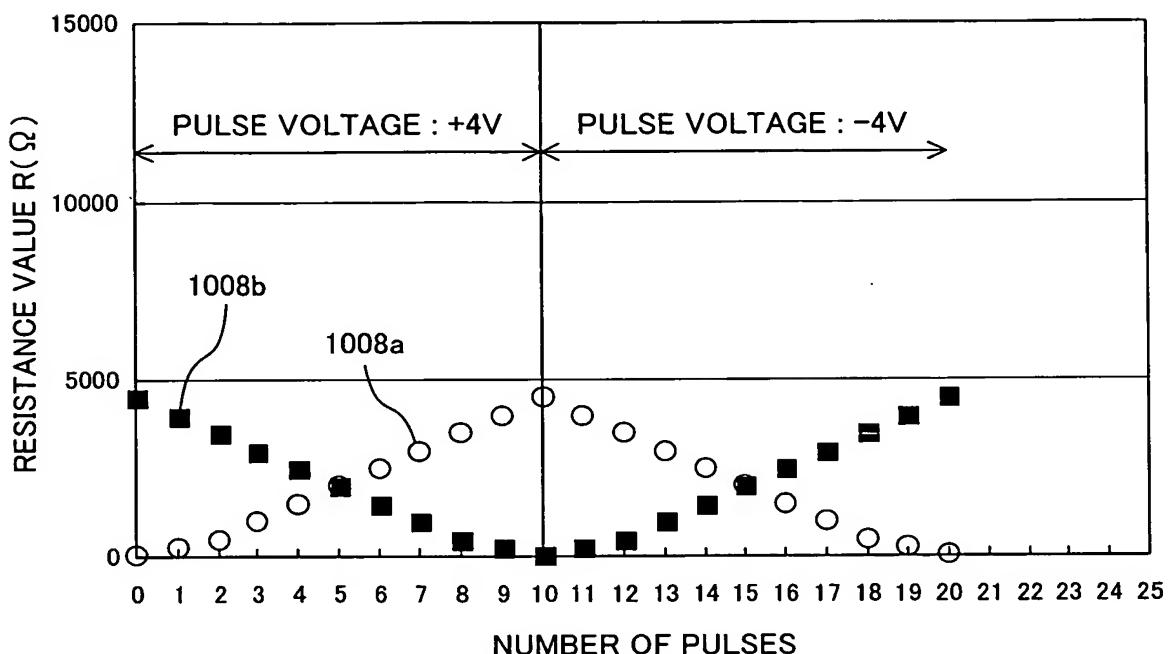


FIG. 12

(a) RESISTANCE CHANGE WITH NUMBER OF PULSES



(b) OUTPUT VOLTAGE IN READOUT OF RECORDING STATE

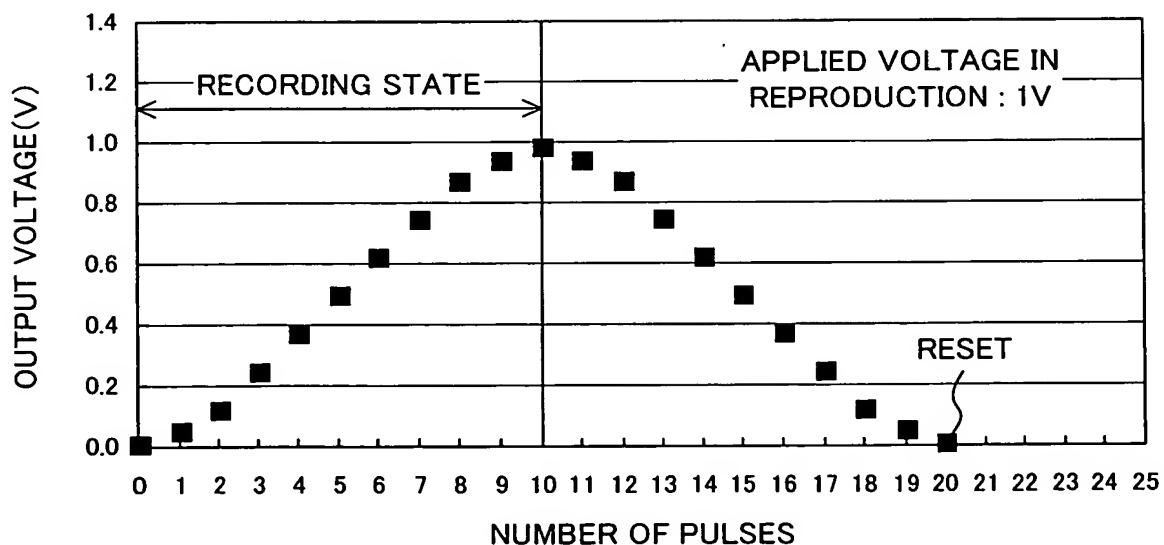


FIG. 13

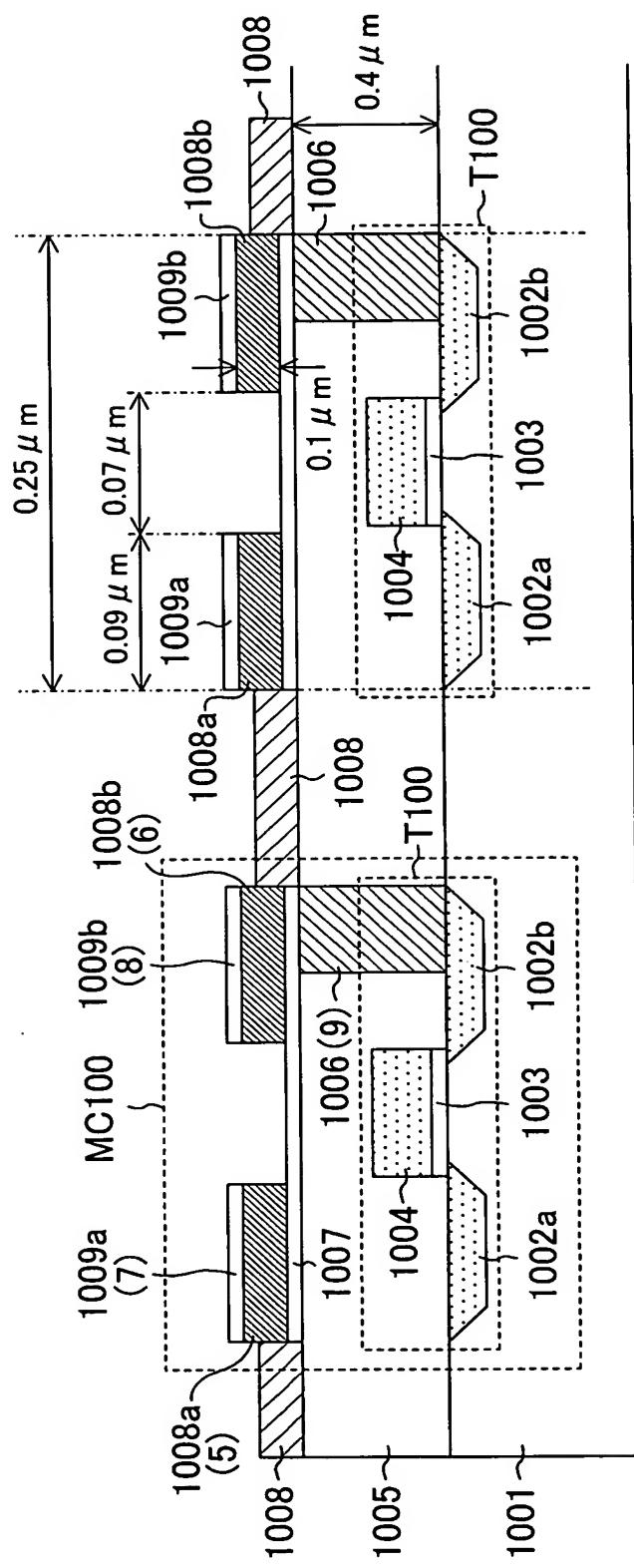


FIG. 14

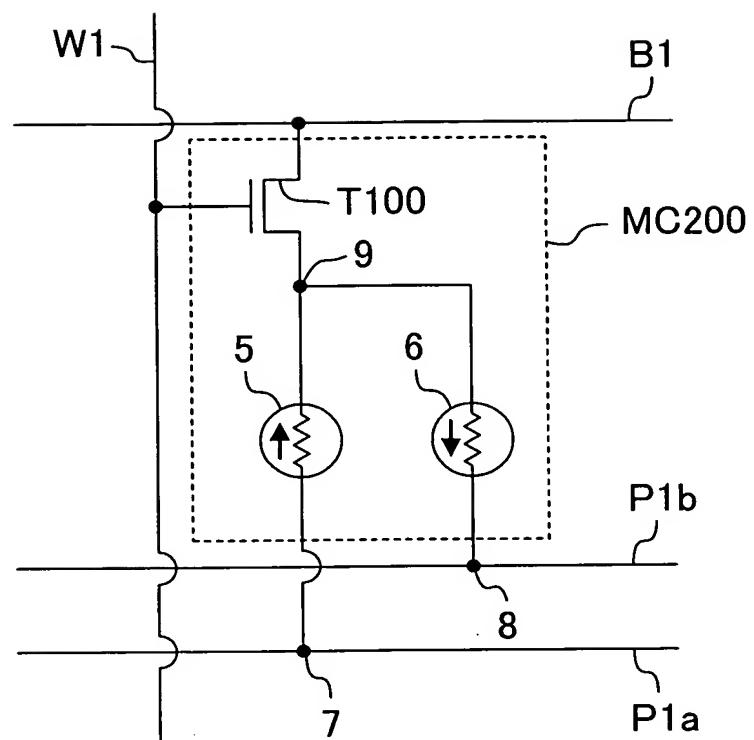
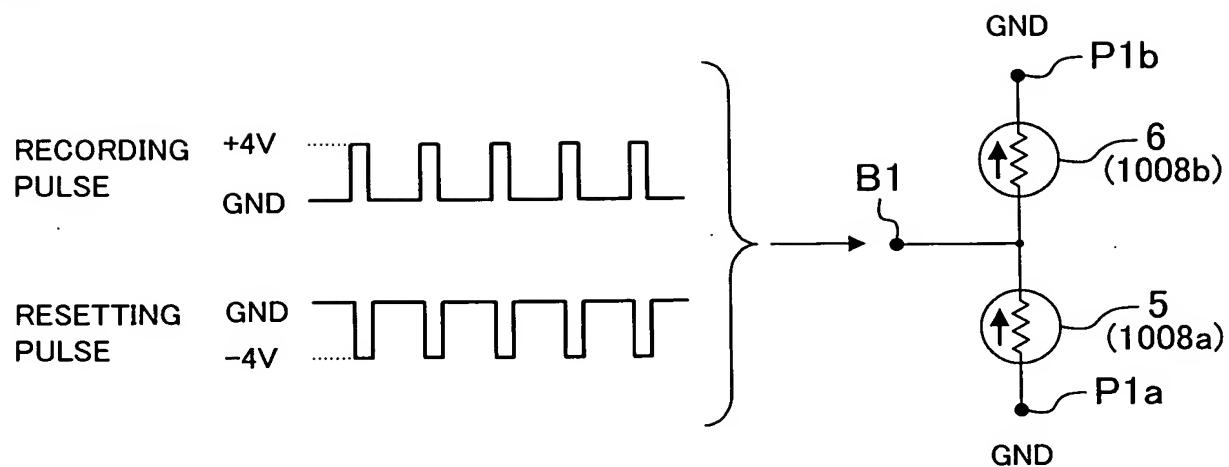
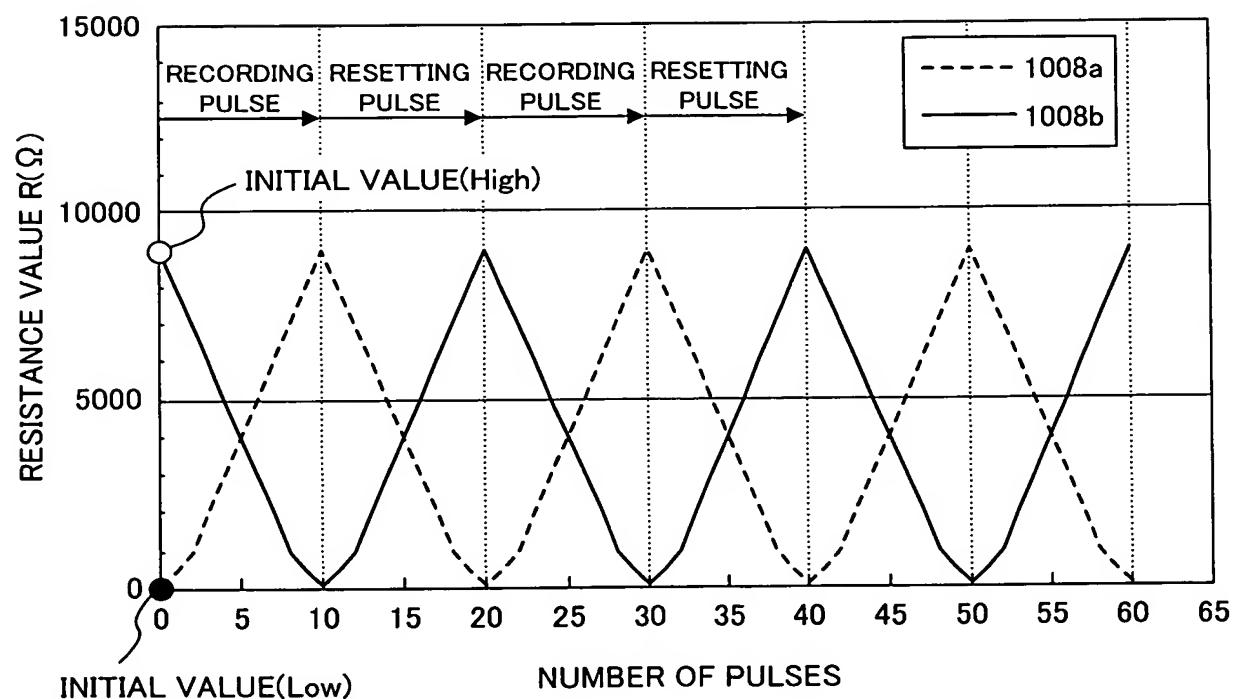


FIG. 15

(a)



(b)



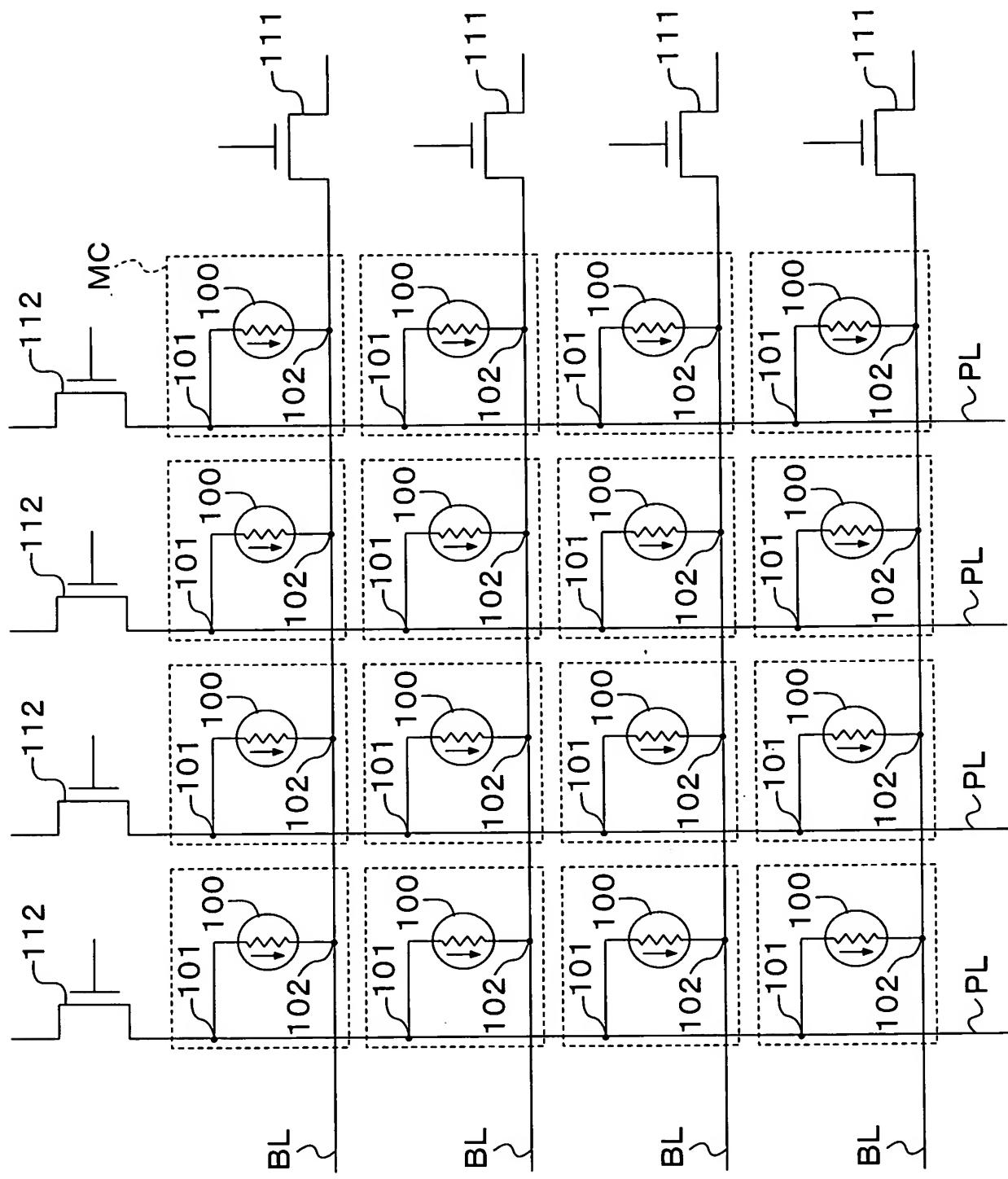
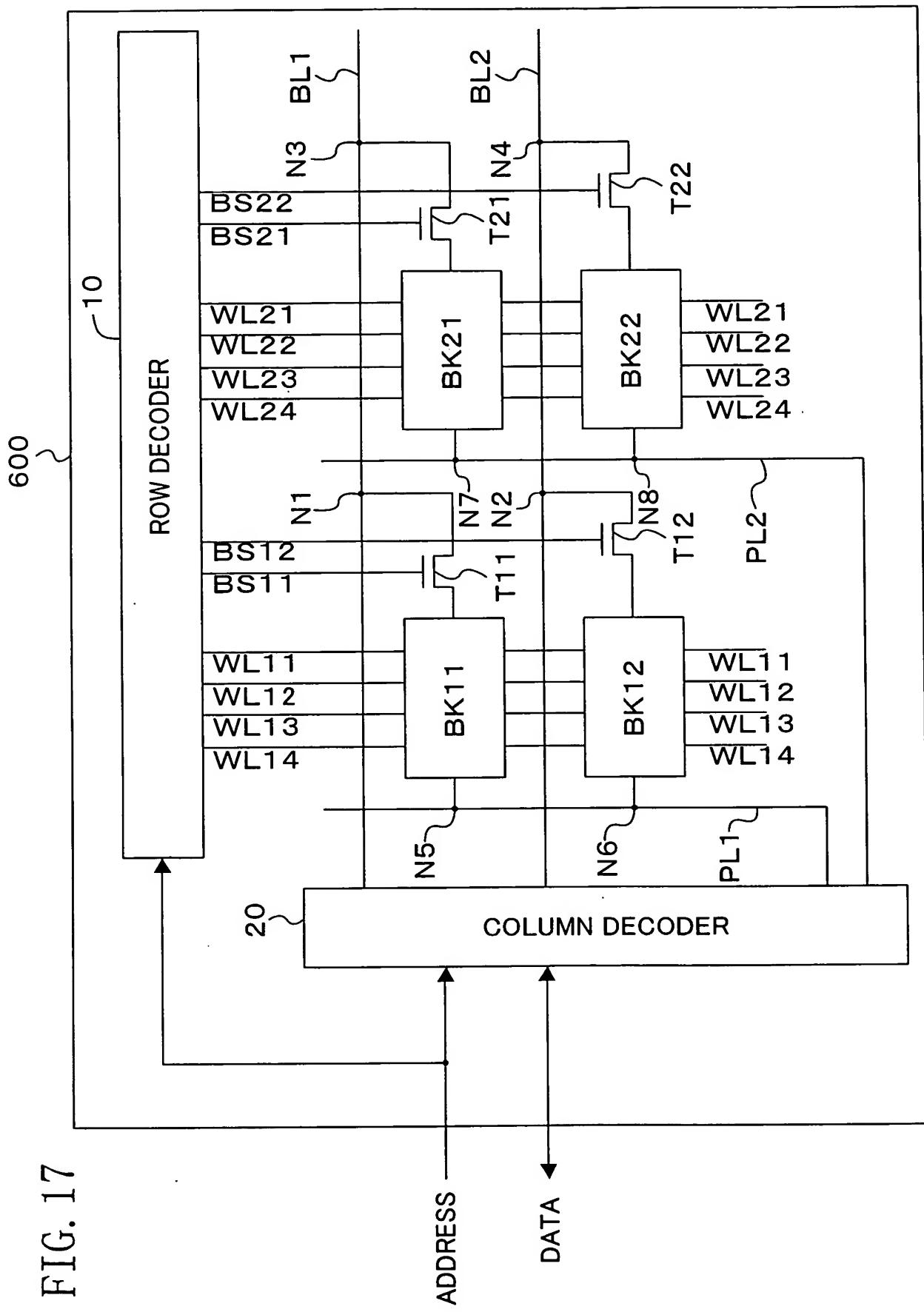


FIG. 16



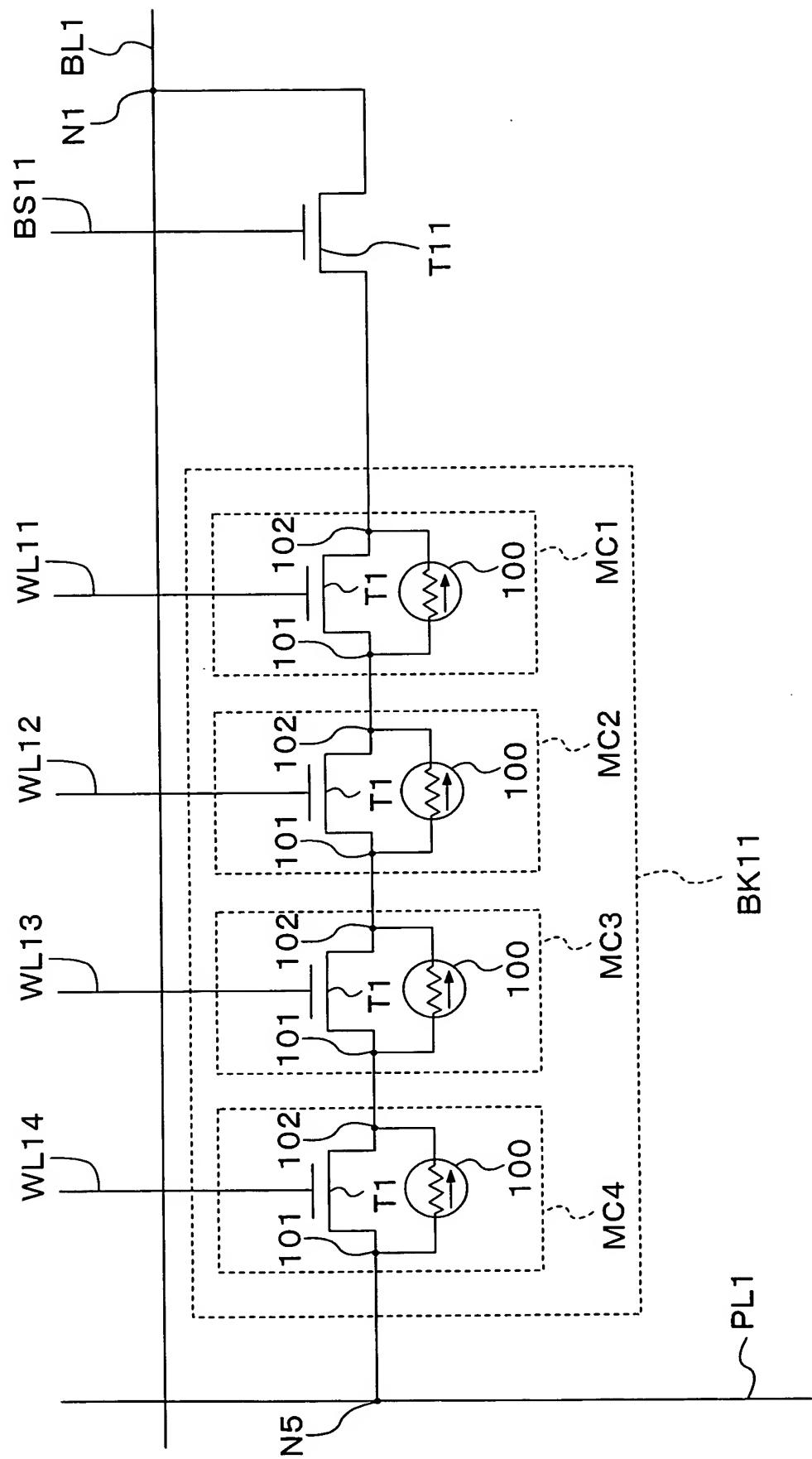
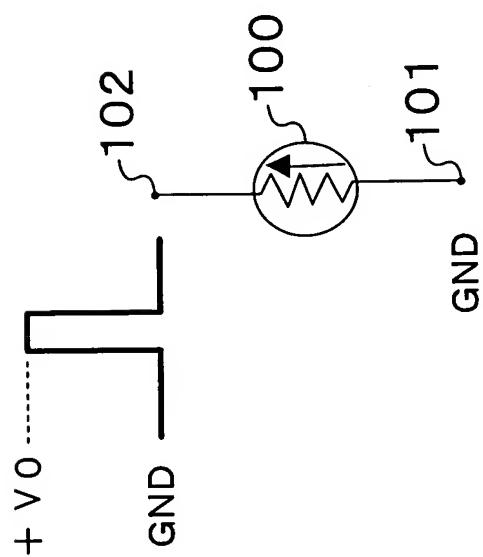
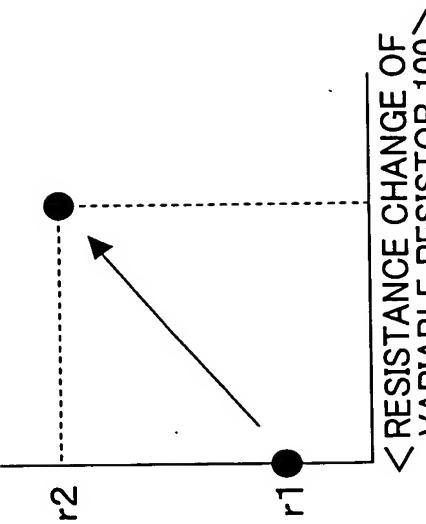


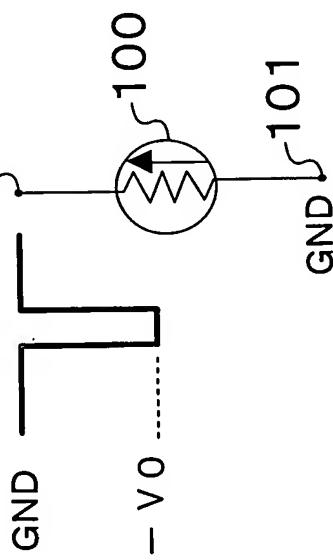
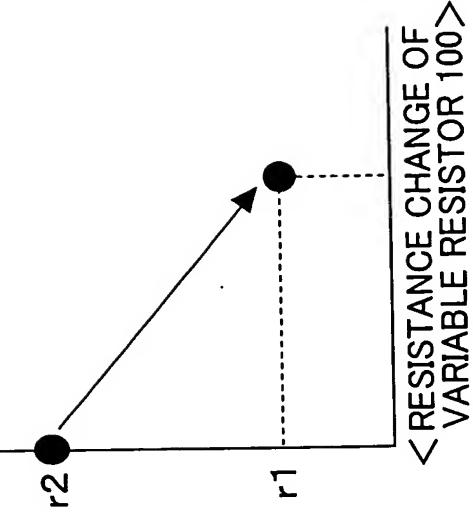
FIG. 18

FIG. 19

(a) POSITIVE PULSE

RESISTANCE
VALUE R <RESISTANCE CHANGE OF
VARIABLE RESISTOR 100>

(b) NEGATIVE PULSE

RESISTANCE
VALUE R <RESISTANCE CHANGE OF
VARIABLE RESISTOR 100>

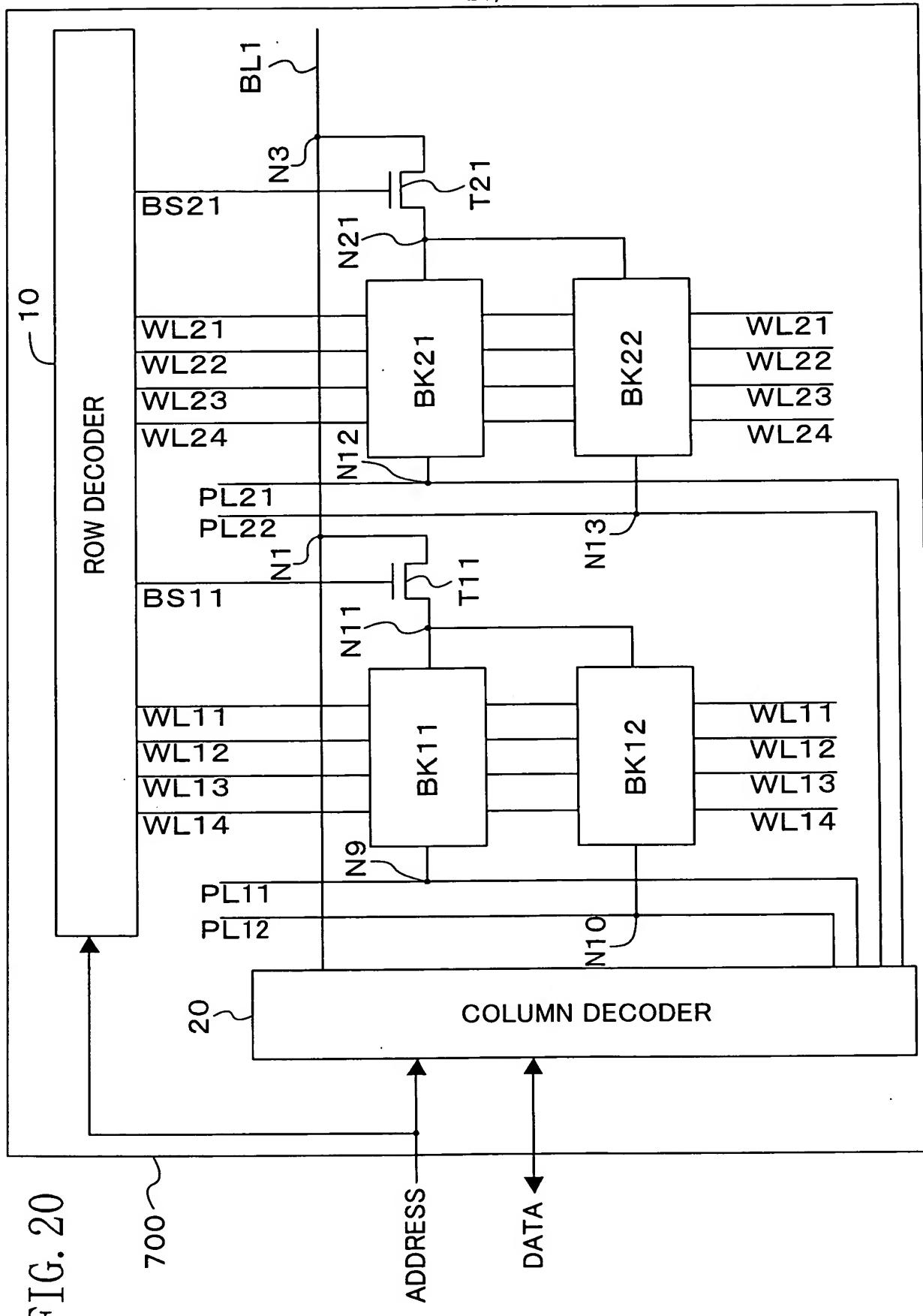


FIG. 20

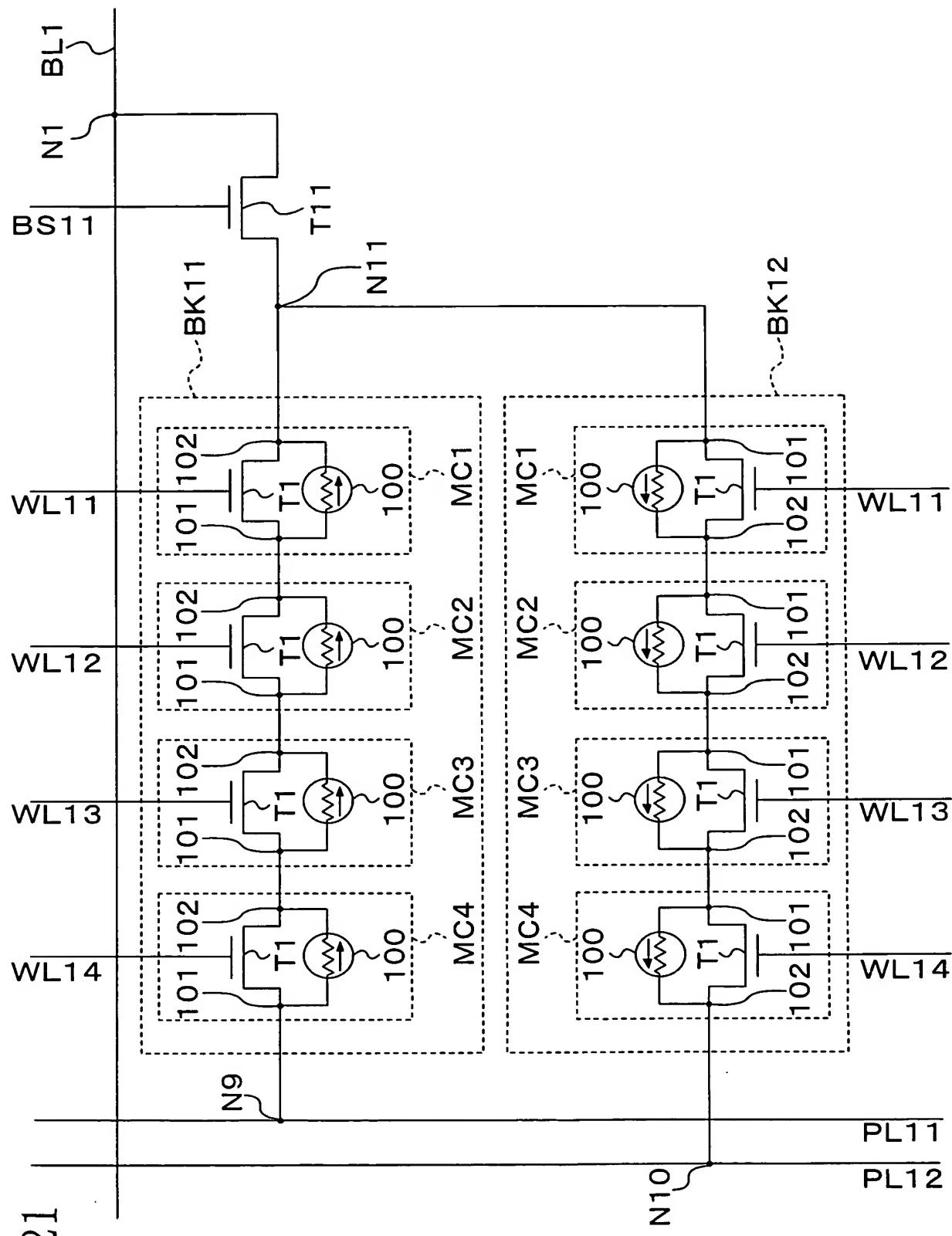


FIG. 21

FIG. 22

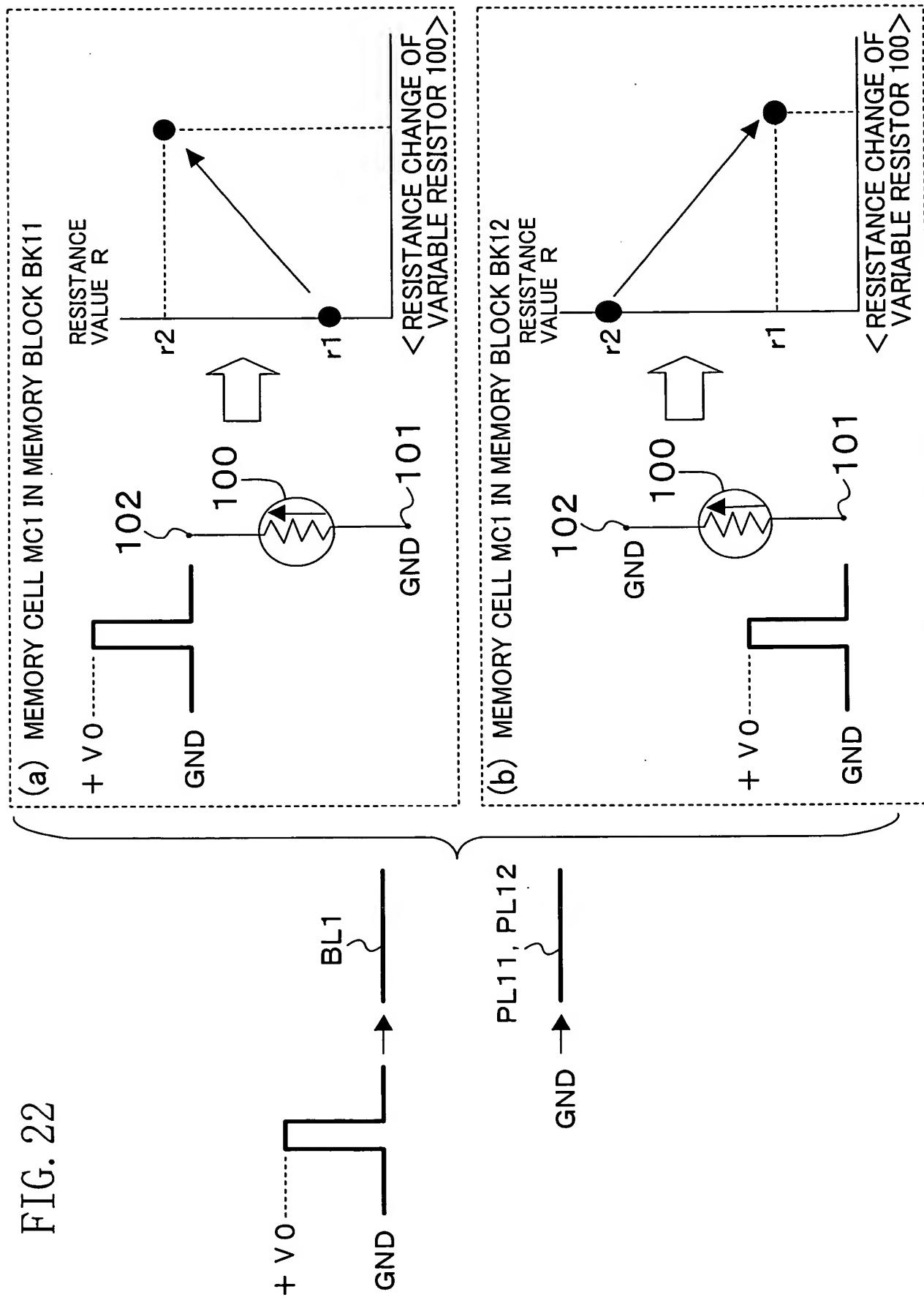


FIG. 23

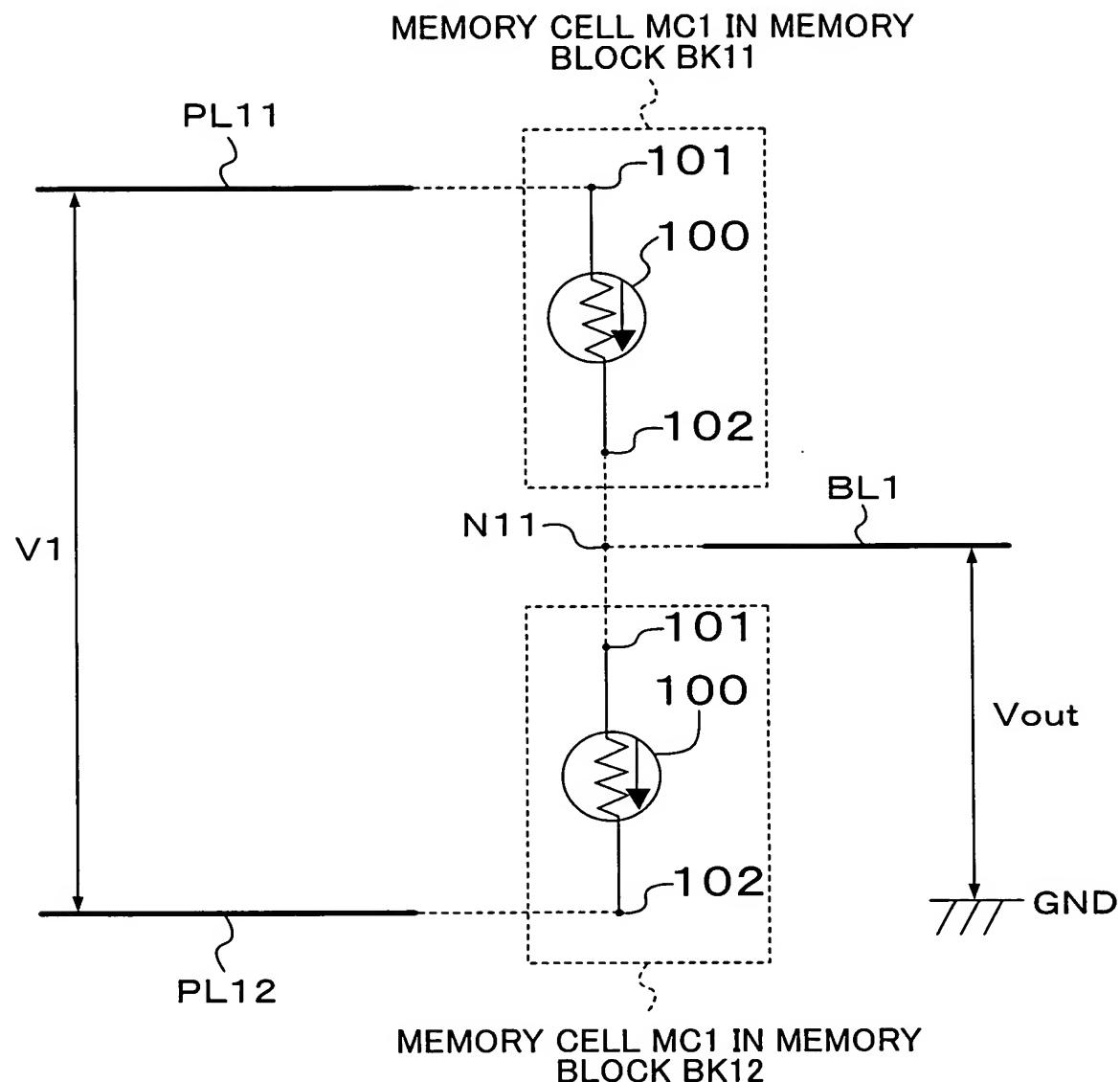
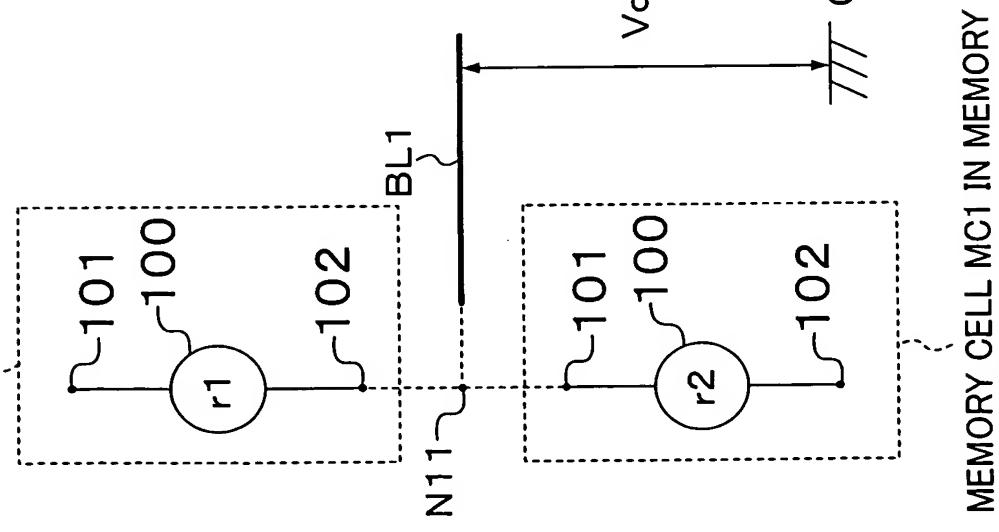


FIG. 24

(a) READOUT OF DATA "0"
MEMORY CELL MC1 IN MEMORY
BLOCK BK11



(b) READOUT OF DATA "1"
MEMORY CELL MC1 IN MEMORY
BLOCK BK11

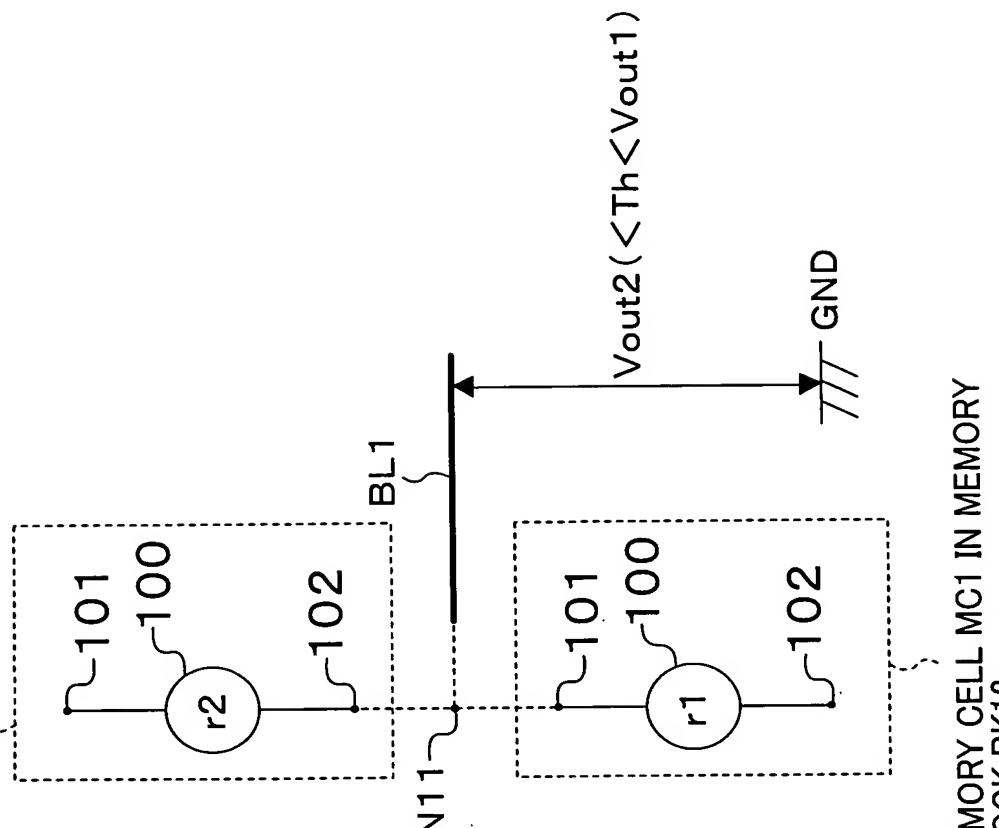
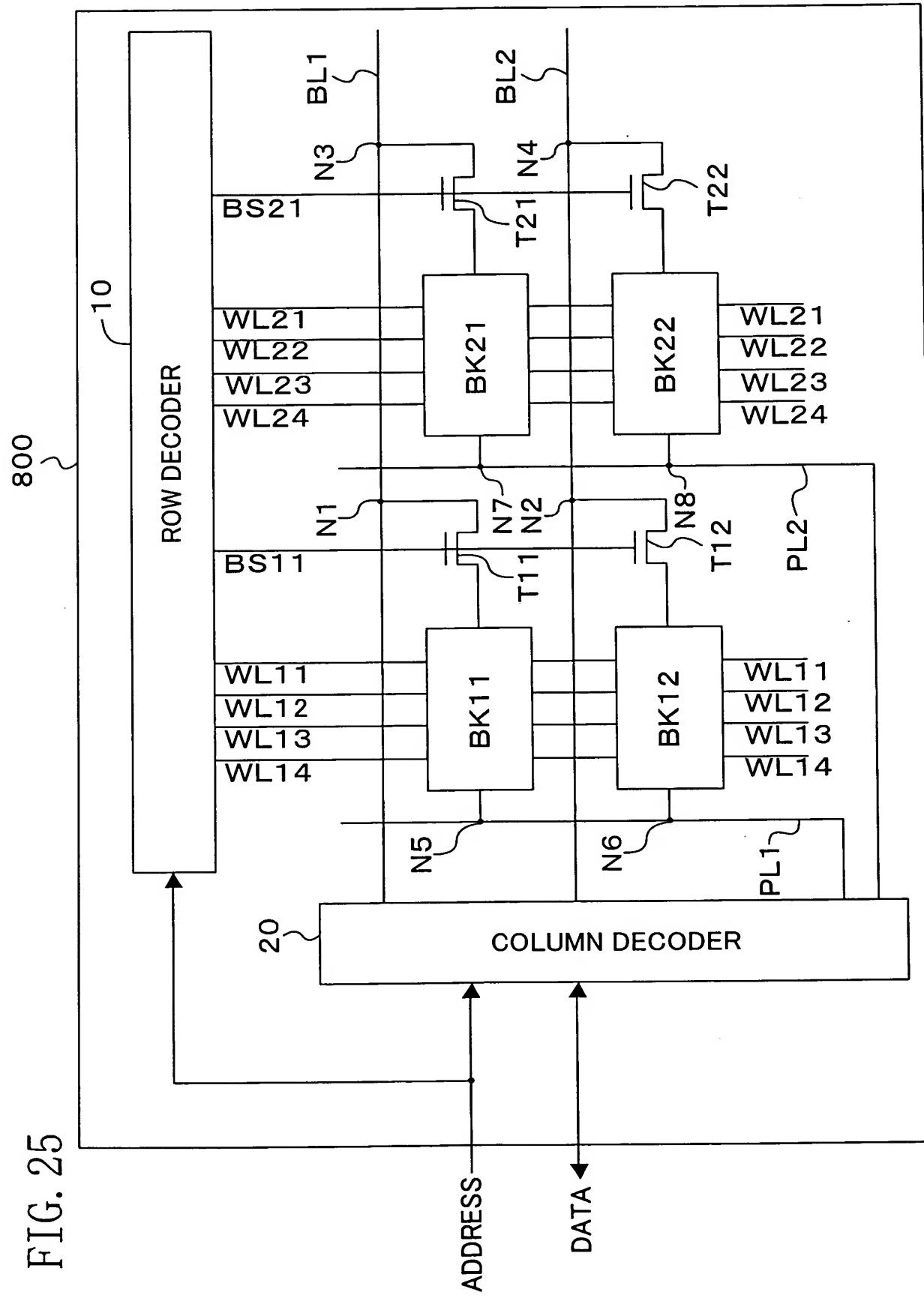


FIG. 25



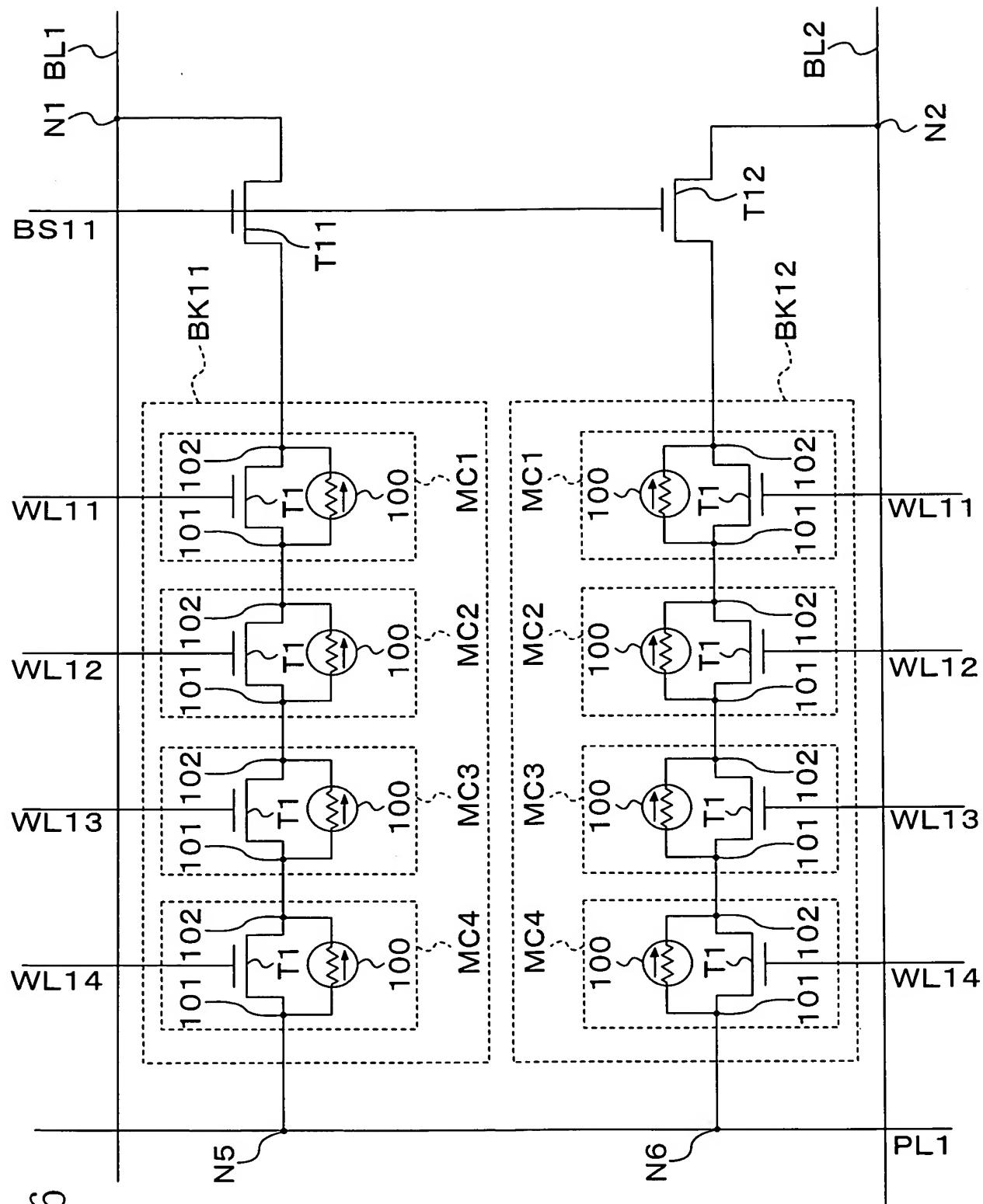


FIG. 27

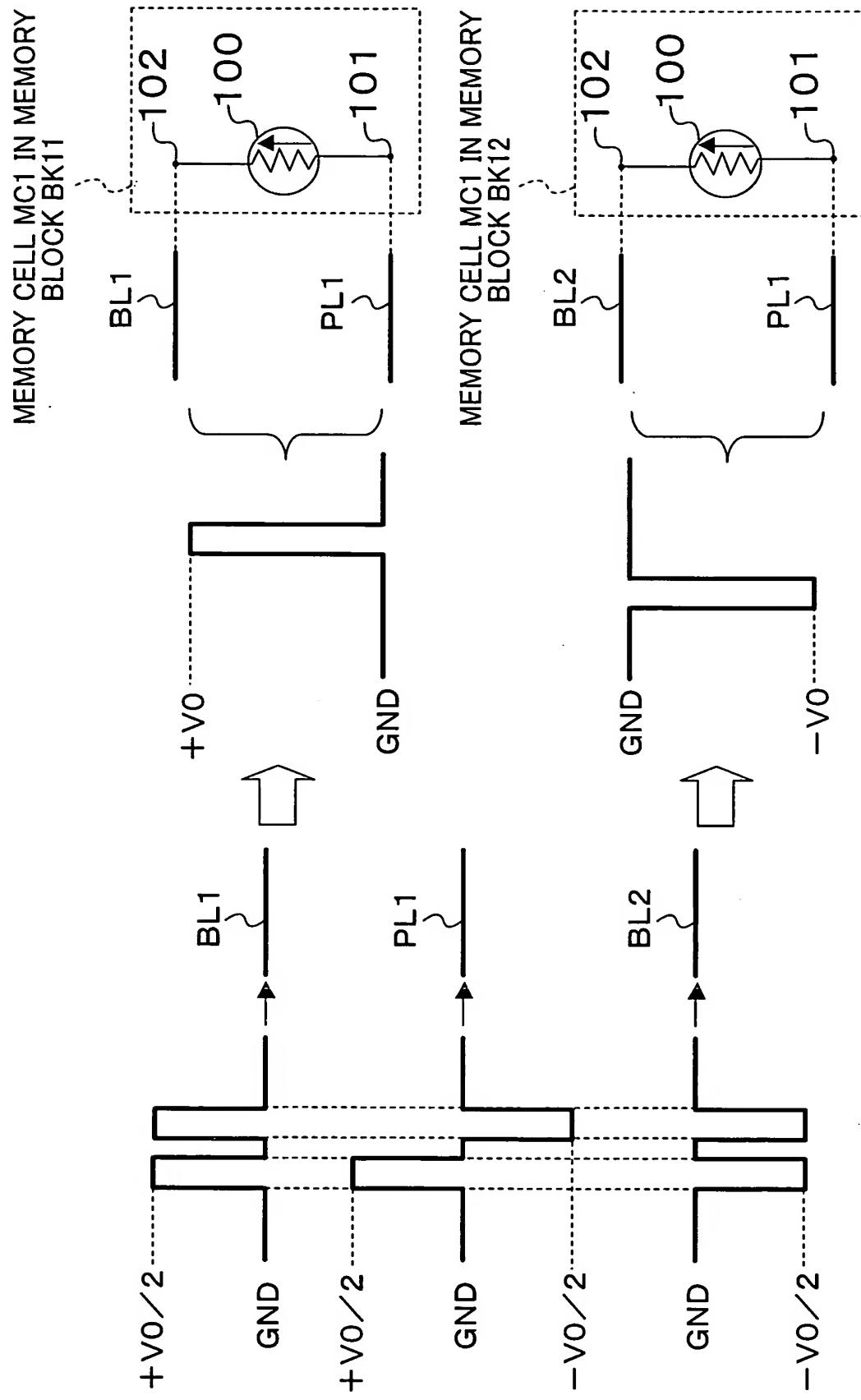
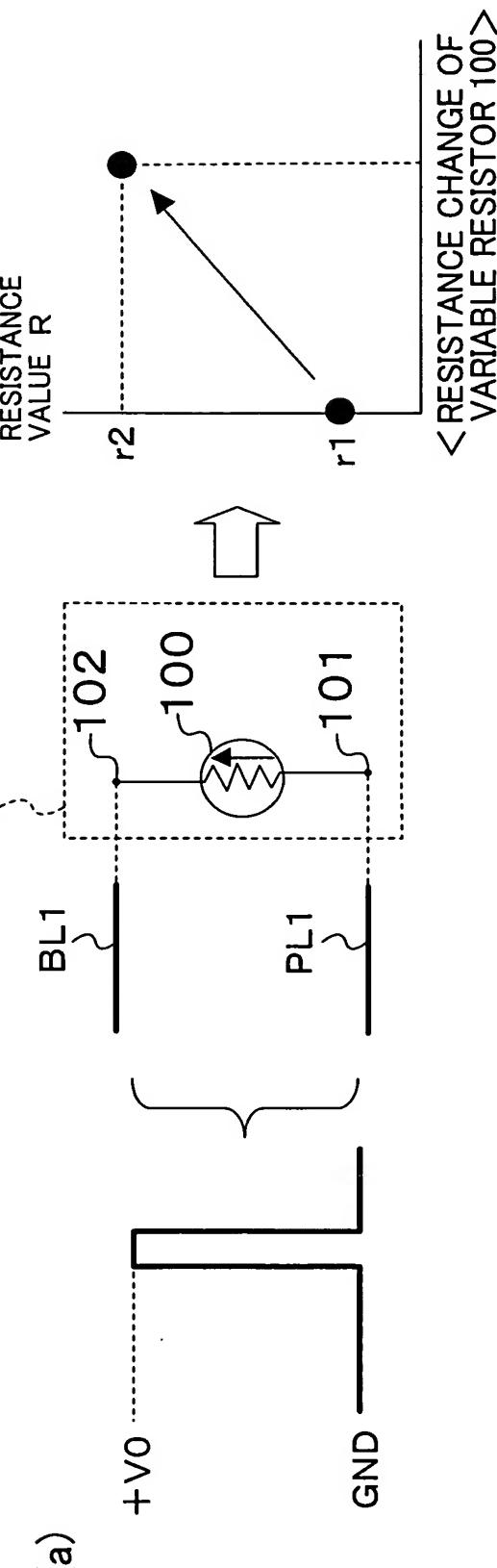


FIG. 28

MEMORY CELL MC1 IN MEMORY BLOCK BK11



MEMORY CELL MC1 IN MEMORY BLOCK BK12

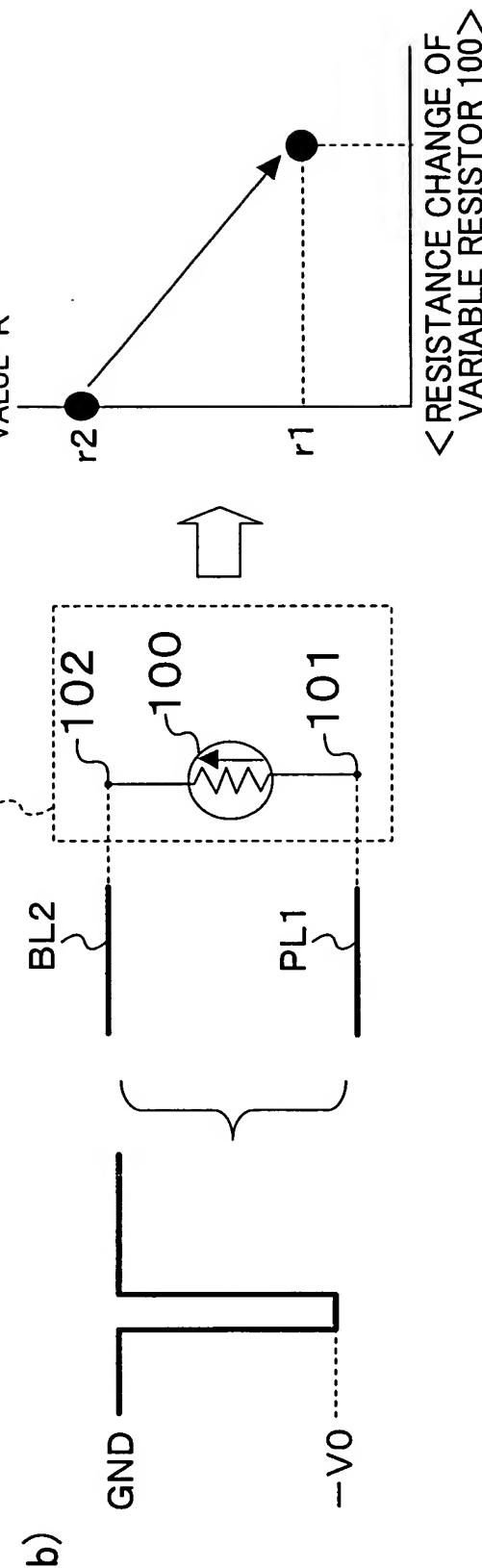
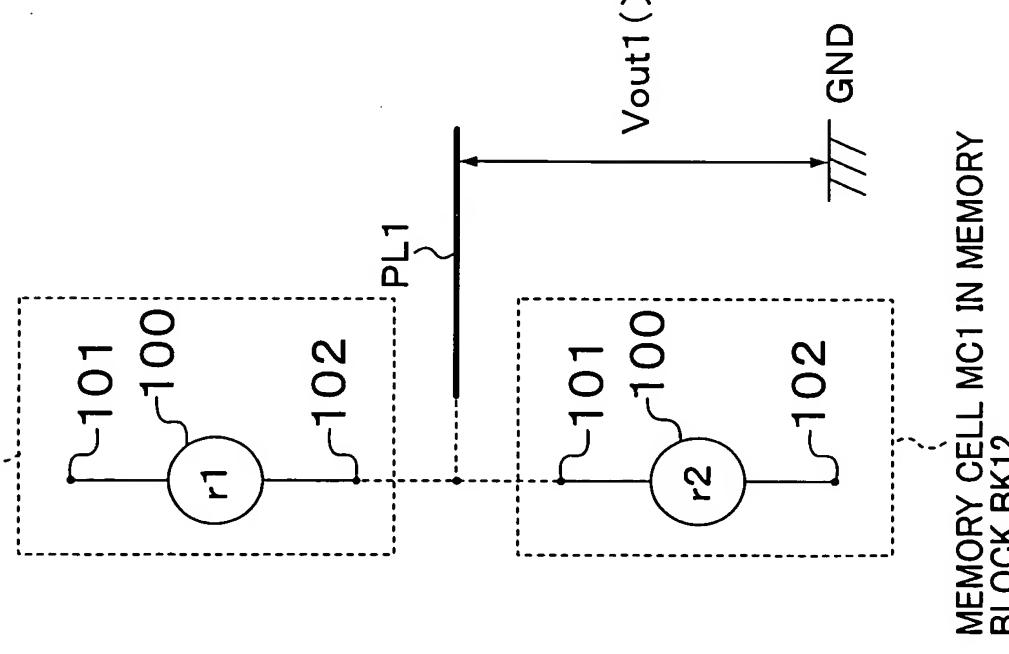


FIG. 29

(a) READOUT OF DATA "0"
MEMORY CELL MC1 IN MEMORY
BLOCK BK11



(b) READOUT OF DATA "1"
MEMORY CELL MC1 IN MEMORY
BLOCK BK11

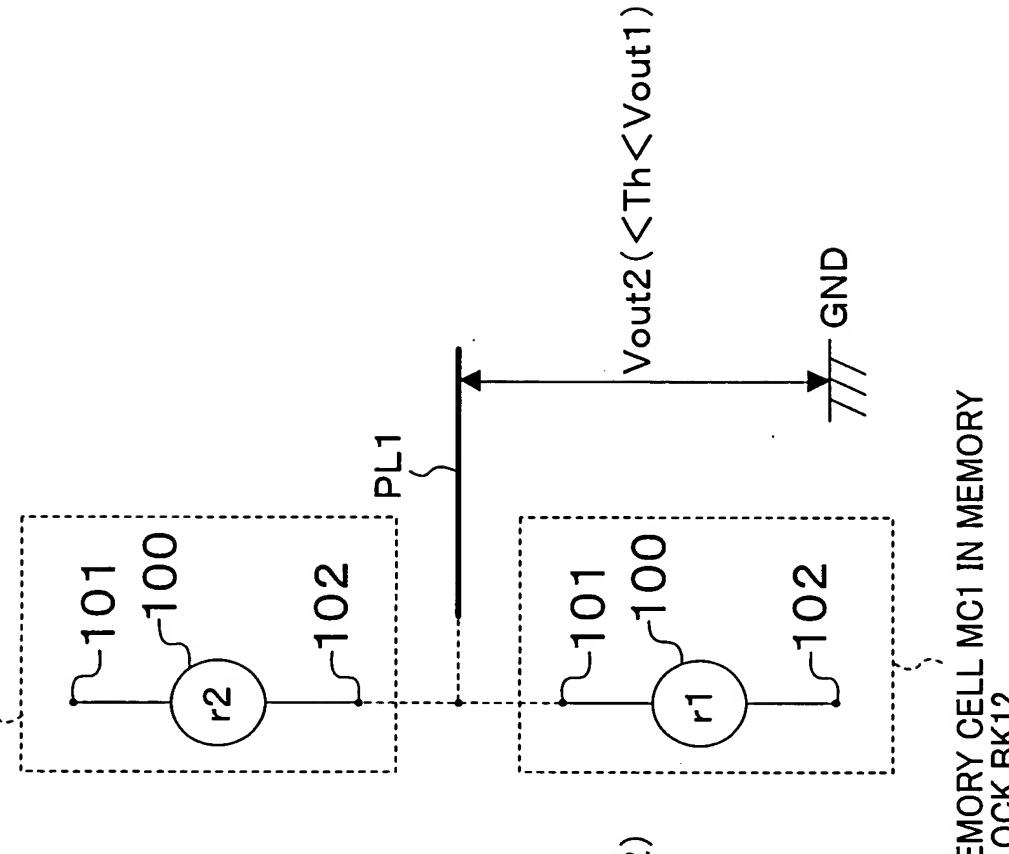


FIG. 30

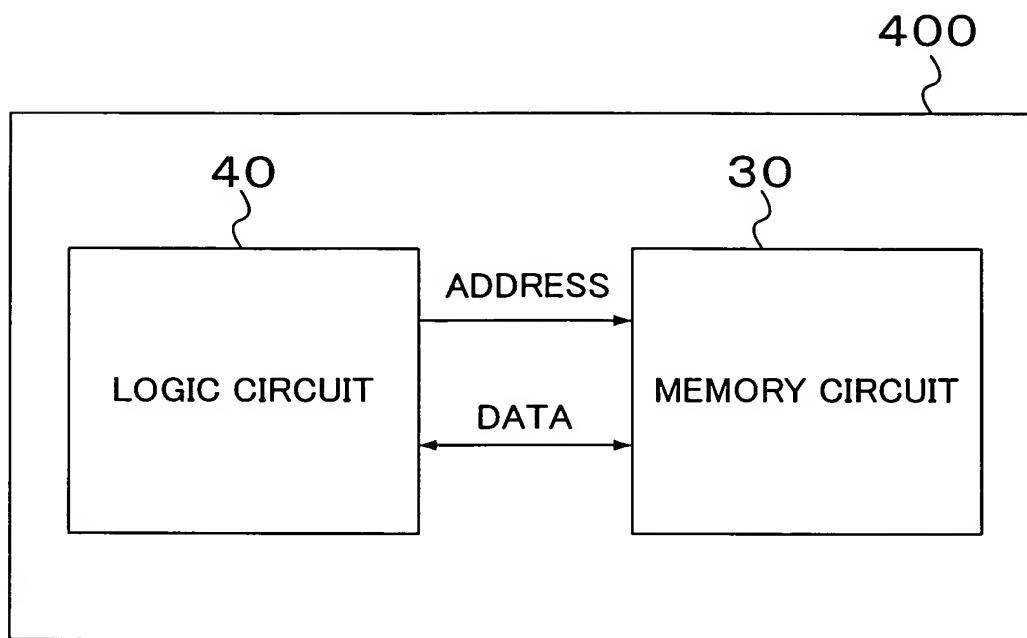


FIG. 31

